High-Frequency Low-Power IC's in a Scaled Submicrometer HBT Technology

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***Abstract*—Fast, dense, and low-power integrated circuits (IC's) have been developed using a new scaled heterojunction bipolar transistor (HBT) IC process. HBT's have been fabricated with emitter dimensions of 0.3 μm^2 and a circuit metallization pitch of 4 μm to reduce power and compact the chip size. Submicrometer HBT's exhibited f_T of over 160 GHz. A number of circuits using this new technology have been demonstrated, including a low-power comparator test chip clocked at 40 GHz and an ultra-low-power phase-locked-loop-based (PLL) clock and data-recovery circuit consuming 22-mW dc power at 4 GHz.**

***Index Terms*— CDR, comparator, HBT, HBT scaling, high-frequency IC's, InP, low-power IC's, PLL.**

I. Introduction

HETEROJUNCTION bipolar transistor-based (HBT) integrated circuits (IC's) have shown potential for large-scale integrated (LSI) levels of integration. HBT's are attractive in three product areas: wireless communications, high data-rate optical communications, and data conversion. In wireless applications, the trends are toward low-voltage low-power electronics to increase the battery life and reduce the weight of portable units. In other applications, power consumption will be a major limitation of HBT IC's for high-speed performance. Generally the RF characteristics of an HBT peak at current densities of around 10^5 A/cm^2. To fully utilize this performance potential while keeping the dc power consumption under control, the device dimensions must be scaled down to submicrometer dimensions. An additional advantage of submicrometer HBT devices is their low thermal resistance compared to larger devices. This allows small transistors to operate at current densities in excess of 10^6 A/cm^2, thus reaching their electronic limits of conduction.

In this paper, we have demonstrated fast, dense, and low-power IC's using a newly developed scaled HBT IC technology on an InP substrate. The new fabrication technique allows us to make devices with emitter dimensions as small as 0.3 μm^2. We have been able to achieve low circuit power consumption by utilizing the HBT's with an emitter dimension of 0.5 μm^2 in a number of demonstration circuits. This is a significant reduction in the emitter area of transistors compared to our baseline HBT IC technology [1], [2]. To achieve chip area compaction, we have reduced the interconnect metallization pitch from the original 8 μm in our baseline process down to 4 μm. The submicrometer HBT's exhibited f_T values of greater than 160 GHz and dc current gain of greater than 50. Using this new process, we have demonstrated circuits including a clock and data recovery (CDR) chip and a comparator test chip clocking at 40-GHz frequency. A phase-locked-loop–based (PLL) CDR architecture was used which included a digital phase detector and a multivibrator-type voltage-controlled oscillator (VCO). At 4 GHz, the fully functional chip consumed a total of 50-mW dc power including input and output buffers from a single supply of -2.5 V. The CDR power consumption excluding input/output buffers was 22 mW. A comparator test chip was also demonstrated comprising a clock driver, master–slave latching comparator, output buffer, and bias generator. Each comparator cell comprising 21 transistors consumed approximately 25-mW dc power from a single 3.2-V negative supply. The comparator is a key building block and speed limiter of parallel or flash architecture analog-to-digital converters (ADC's). Parallel ADC's require 2^n comparators for n-bit accuracy.

This paper begins with a description of the new fabrication technology including a detailed process flow. Next, transistor dc and RF performance are presented including $I_C - V_{CE}$, f_T, and $f_{\max}$ characteristics. Two examples of demonstrated circuits are presented in detail including transistor-level circuits and performance results. First we will present a comparator test chip including 90 submicrometer HBT's. Finally we will describe a low-power PLL-based clock and data-recovery circuit comprising 97 submicrometer HBT's.

II. Fabrication Technology

The molecular beam epitaxy (MBE) grown epitaxial profile of fabricated HBT's is shown in Fig. 1. The emitter cap layer in this profile was 0.4 μm to accommodate metallization contact to the emitter terminal of the device. A schematic cross-sectional view of the scaled HBT IC process is shown in Fig. 2. In this process, we defined very fine emitter geometries into a thin layer of silicon nitride which acted as a mask to remove the n^+ emitter cap layer by reactive ion etching (RIE) techniques [see Fig. 2(a)]. Subsequently, we formed a sidewall by depositing SiO_2 and removing it using RIE. In the next fabrication step, this SiO_2 sidewall formed overhangs [shown in Fig. 2(b)] when we removed the n-emitter by wet chemical etching. A single metallization step then defined both the emitter and base ohmic contacts [see Fig. 2(c)]. Base-collector mesa, collector ohmic, and isolation mesa followed as shown in Fig. 2(d) and (e). At this point in the process we fabricated resistors, capacitors, and first interconnect metal layers [see Fig. 2(e)]. Final stages of the process are shown

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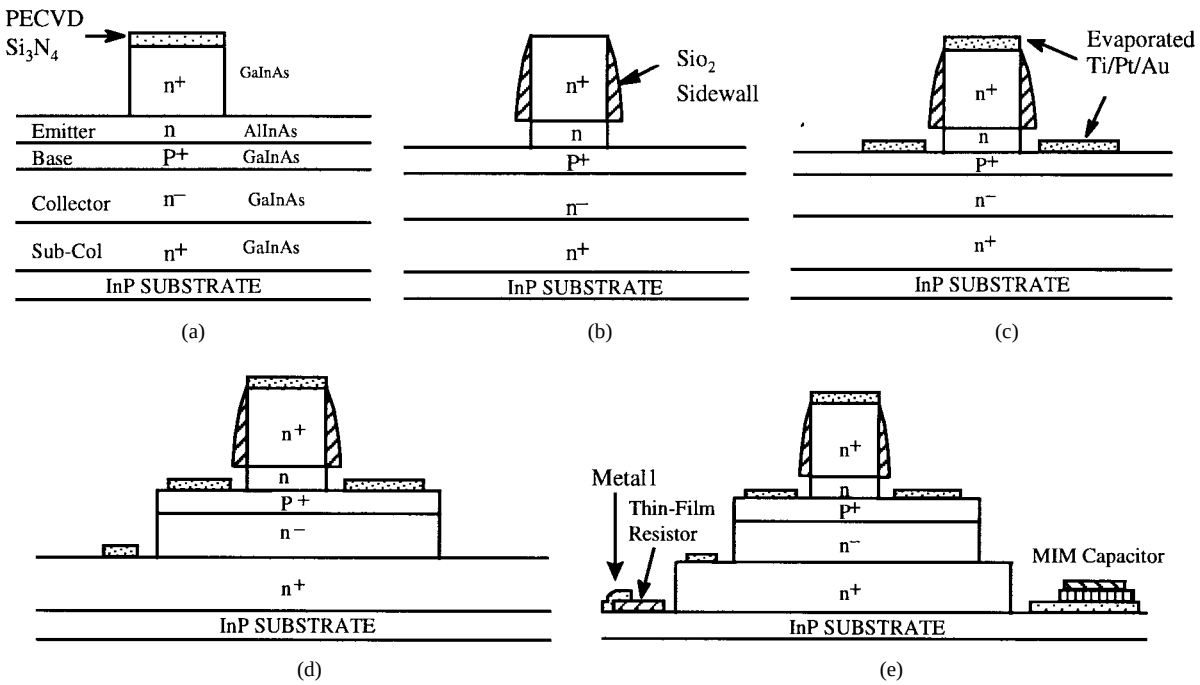


Fig. 1. Schematic fabrication steps for the submicrometer self-aligned HBT process.

400 nm	GaInAs Contact	$n = 1x10^{19}$ cm^{-3}
20 nm	AlInAs Emitter Contact	$n = 1x10^{19}$
70 nm	AlInAs Emitter	$n = 8x10^{17}$
30 nm	9-Period AlInAs/GaInAs Superlatice Graded Region 23.3 nm $n = 8x10^{17}$ 6.7 nm $p = 2x10^{18}$	→ Period 9 (3.3 nm) (3.3 nm) Period 1 →
10 nm	GaInAs Spacer	$p = 2x10^{18}$
40 nm	GaInAs Base	$p = 2.6x10^{19}$
300 nm	GaInAs Collector	$n = 5x10^{15}$
350 nm	GaInAs Subcollector	$n = 1x10^{19}$
10 nm	GaInAs Buffer	Undoped
	InP Substrate	

Fig. 2. MBE grown epitaxial profile of scaled InP-based HBT.

in Fig. 2(f). In the final steps, we planarized the wafer with polyimide, etched back the polyimide to expose emitter tops, etched via holes by RIE, and patterned second metallization layer for global circuit interconnection.

Using this new process, we have been able to successfully fabricate HBT's with emitters as small as 0.2 μm^2. This is a factor of 20 reduction in the emitter area of transistors compared to our baseline minimum geometry HBT which was 2×2 μm^2.

III. Transistor Characteristics

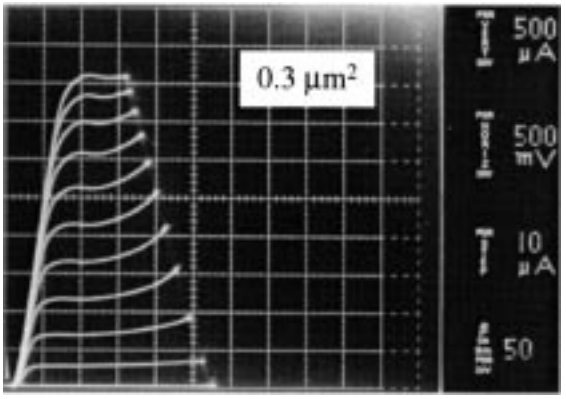
I–V characteristics of a typical 0.3 and 0.5 μm^2 HBT is shown in Fig. 3 exhibiting a dc current gain of over 50 for a submicrometer transistor. Furthermore, this device can carry a collector current density of greater than 10^6 A/cm^2, as seen in Fig. 3. Ultimately, the collector current in these devices is limited by collector conductivity modulation also known as the Kirk effect. This is seen in the *I–V* characteristics as a compression of current gain at current densities in excess of 10^6 A/cm^2. Generally a large area HBT will not reach this electronic limit of conduction because it will reach the thermal limit due to excessive self heating. The small-area HBT's exhibited negligible thermal resistance resulting in collector current conduction to be electronically limited.

The RF performance of the scaled HBT is shown in Figs. 4 and 5 where we have plotted the unity gain cutoff frequency f_T and maximum frequency of oscillation $f_{\max}$ as a function of collector current, respectively. These measurements were done at a collector–emitter voltage of 1.25 V. We measured higher values of f_T and $f_{\max}$ at V_{CE} of 1.5 and 1.75 V. As seen in these figures, the transistor exhibited an RF performance of greater than 40 GHz at 100 μA of collector current while the peak values of f_T and $f_{\max}$ occurred at around 1 mA. There is no significant size dependence evident from these figures for transistor dimensions down to 0.3 μm^2. Devices with an emitter geometry of 0.2 μm^2 exhibited noticeable reduction in both f_T and $f_{\max}$, indicating the limit of device scaling for InP-based HBT's.

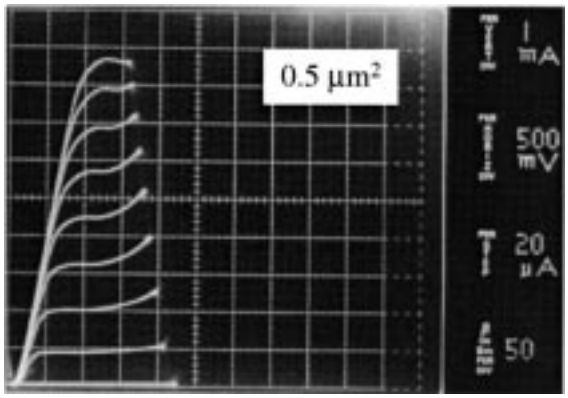
IV. Circuit Implementation

A. Latching Comparator

Using this new process, we have demonstrated a comparator test chip comprising two cascaded master–slave comparators, a preamplifier, a bias generator, a clock driver, and an output buffer—a total of 90 transistors. A block diagram of the test chip is shown in Fig. 6. All the circuitry were designed in



(a)



(b)

Fig. 3. Measured *I–V* characteristics of two typical HBT's with (a) 0.3-μm^2 emitter size and (b) 0.5-μm^2 emitter.

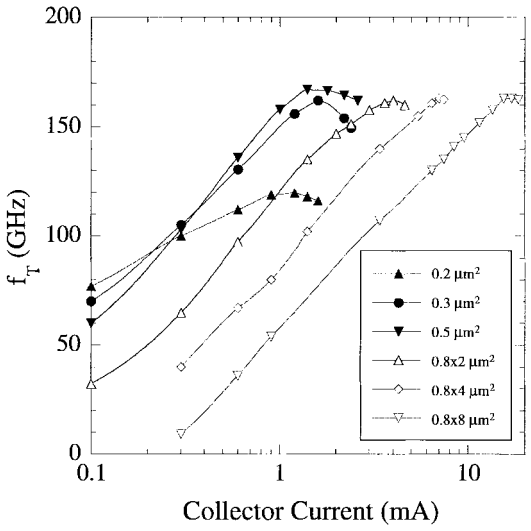


Fig. 4. Measured unity-gain cutoff frequency f_T as a function of collector current for different size HBT's.

a fully differential architecture for maximum speed advantage. A simplified schematic of the comparator is shown in Fig. 7. The comparator featured split-load resistors for improved speed performance. Additional current sources I_2, which were a small fraction of I_1, maintain the comparator differential pairs slightly biased for faster regeneration during

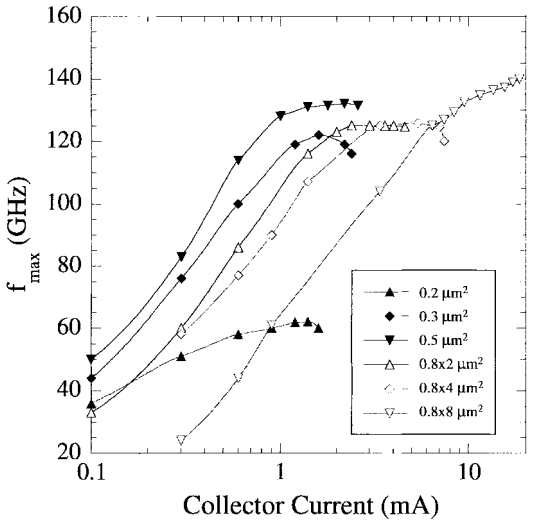


Fig. 5. Measured maximum frequency of oscillation $f_{\max}$ as a function of collector current for different size HBT's.

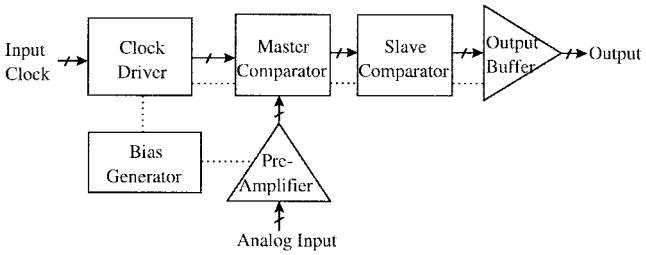


Fig. 6. Block diagram of a master–slave comparator test chip with 90 transistors designed with 0.5-μm^2 emitter HBT's.

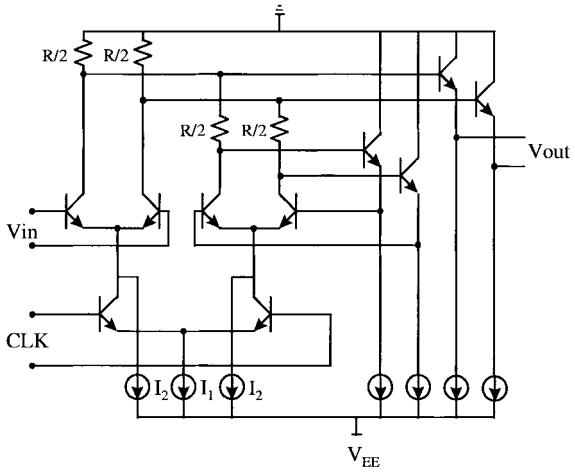


Fig. 7. Simplified schematic of latching comparator.

the decision period of the clock cycle. The master–slave comparators (comprising a total of four latch states) were driven by opposite phases of the clock. This improved the ability of comparators to resolve small differential inputs [3]. The preamplifier and the cascaded master–slave comparator set form the key building block of parallel (also known as flash) architecture analog to digital converters. Any reduction in dc power consumption or chip size of the comparator block will have a significant impact on the achievable performance and resolution of flash-type analog to digital converters.

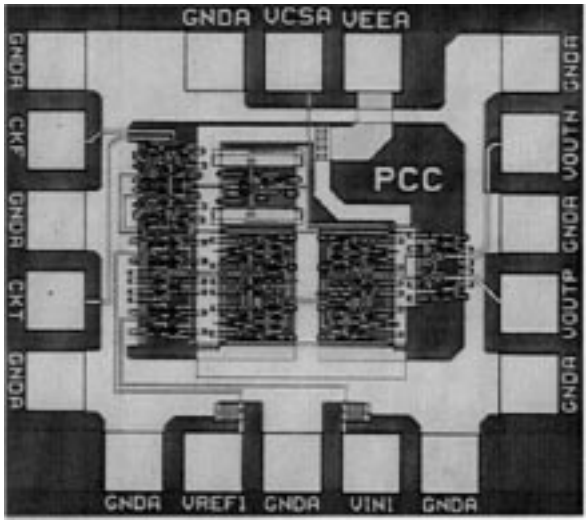
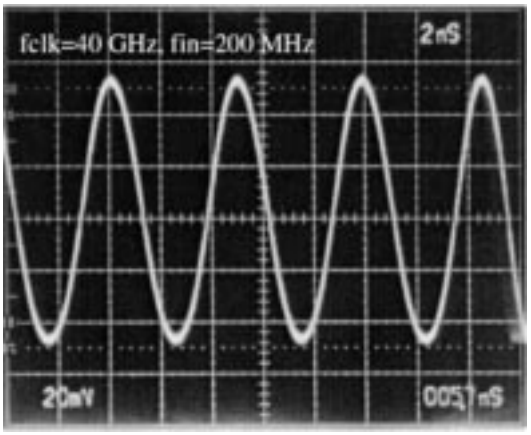


Fig. 8. Die photo of fabricated comparator test chip using scaled 0.5-mm^2 HBT's and a 4-mm metallization pitch.

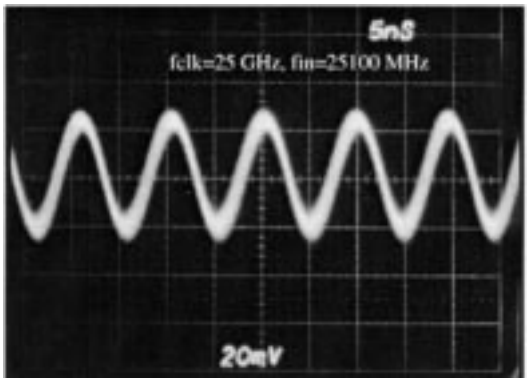
A chip photograph of the fabricated comparator test chip is shown in Fig. 8. The chip was laid out for on-wafer characterization with signal pads adjacent to ground connections. The fabrication process was optimized to significantly reduce the metallization pitch (metal width plus metal-to-metal spacing) from 8 μm in our baseline process down to 4 μm. Correspondingly, the via sizes had to be scaled down to submicrometer dimensions. The reduction in the metallization pitch has a significant effect on compacting the chip size. In complex IC's (such as ADC's), this can potentially reduce the chip size by a factor of four. The size of the comparator test chip reported here was reduced by a factor of approximately three (due to reduction in the metallization pitch and the transistor sizes), compared to a similar layout in our baseline process. This reduction in the chip size will dramatically increase the circuit yield.

The comparator test chip was tested on-wafer using high-frequency probes. The testing was done up to 40 GHz, limited in part by test equipment and the probes. Several different tests were performed on the comparator chip. In all the tests, the comparator was driving an approximately 25-Ω load (50-Ω internal, parallel with a 50-Ω external load). In one test, the comparator input was held at 200 MHz while the clock frequency was increased up to 40 GHz. The comparator output signal at 40-GHz clock frequency is shown in Fig. 9(a). For this test, the input reference voltage was held at zero and one of the two differential outputs were measured. Changing the input reference voltage could change the duty cycle of the output signal, as expected. The frequency performance of the comparator was over three times that of a similar one implemented in our baseline process.

In another test, the comparator was clocked at 25 GHz with an analog input of 25 100 MHz. This test condition generated a beat frequency at 100 MHz (the difference of the clock and input frequencies), as shown in Fig. 9(b). This test indicated that the comparator can operate at an analog input and clock frequency of both 25 GHz. Minimum device size in this comparator design was 0.5 μm^2 and the test chip consumed



(a)



(b)

Fig. 9. Output of comparator test chip driving a 25-Ω load. (a) Clock is at 40 GHz and analog input is at 200 MHz. (b) Beat frequency test of comparator at a clock frequency of 25 GHz and analog input of 25100 MHz.

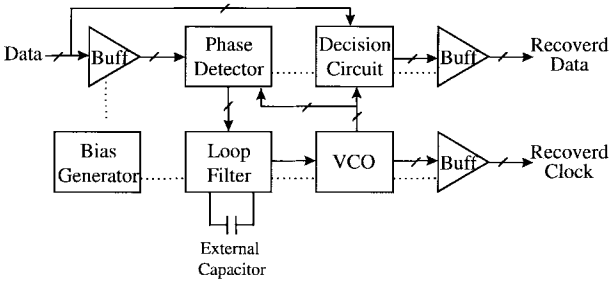


Fig. 10. Block diagram of the single-chip PLL-based CDR circuit.

a total of 176 mW of dc power (supply voltage $= -3.2$ V, supply current $= 55$ mA). This was less than one-third of the power consumed by a similar comparator designed in our baseline process.

B. Clock and Data-Recovery Circuit

The block diagram of the clock and data-recovery circuit is shown in Fig. 10. It consists of input and output buffers, a phase detector, a loop filter, a decision circuit, a VCO, and an on-chip bias generator. A total of 97 HBT's were used in this circuit, the majority of which had an emitter area of 0.5 μm^2. The entire design was fully differential for the speed advantage and immunity from device and process variations.

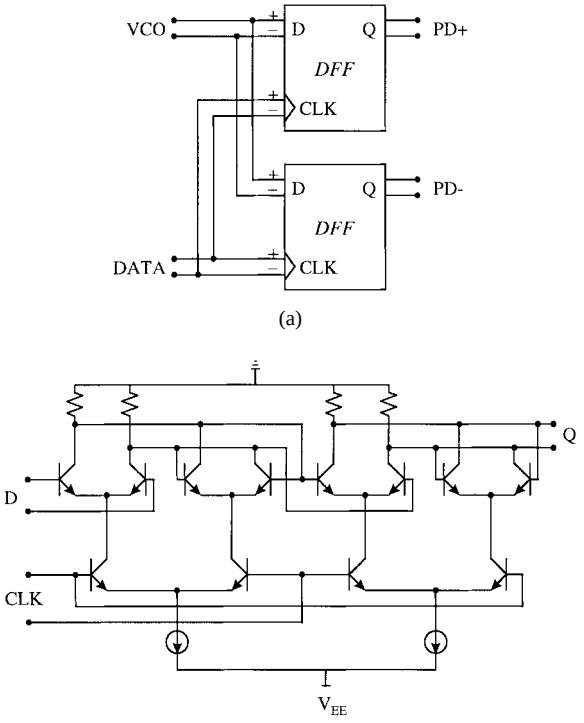


Fig. 11. (a) Block diagram of digital phase detector consisting of two D-type flip-flops. (b) Simplified schematic of the D-type flip-flop used in the phase detector and decision circuit.

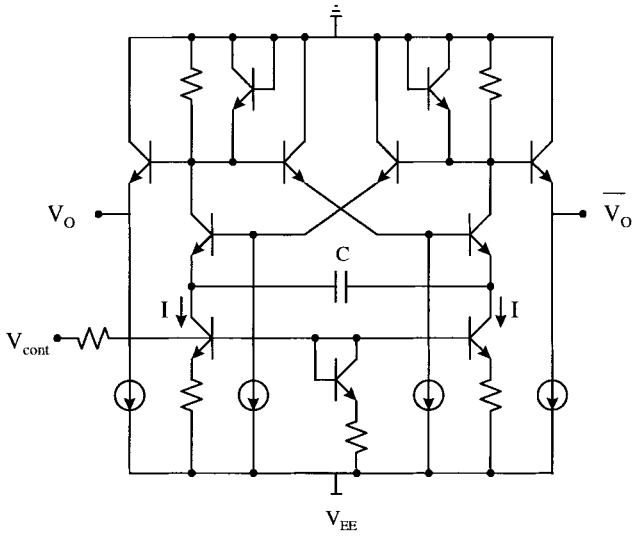


Fig. 12. Simplified schematic of a multivibrator-type VCO with on-chip timing capacitor.

This single-chip clock and data-recovery circuit required only an external capacitor for the loop filter. The CDR employed a PLL-based design [4] including a digital phase detector and decision circuit and a multivibrator-type VCO with an on-chip timing capacitor. The phase-detector portion of the PLL [shown in Fig. 11(a)] was a dual master–slave flip-flop. The dual D-type flip-flop phase detector samples the state of the VCO at both negative and positive transitions of the serial data and results in a nonlinear phase-detector output with three discrete levels. This feature is expected to reduce the VCO

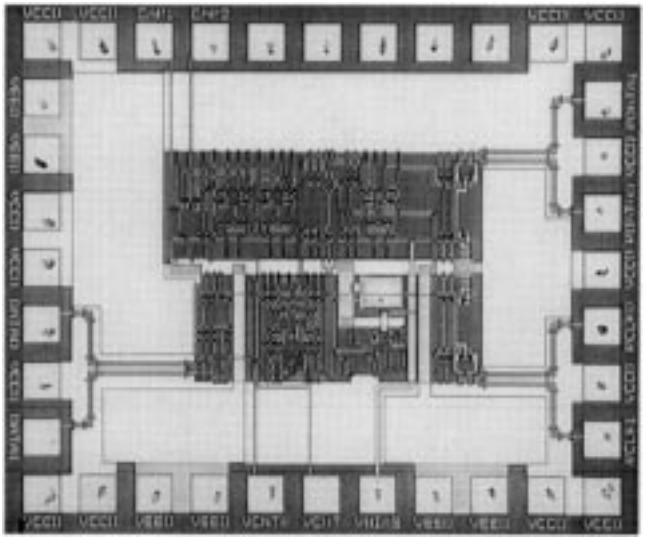
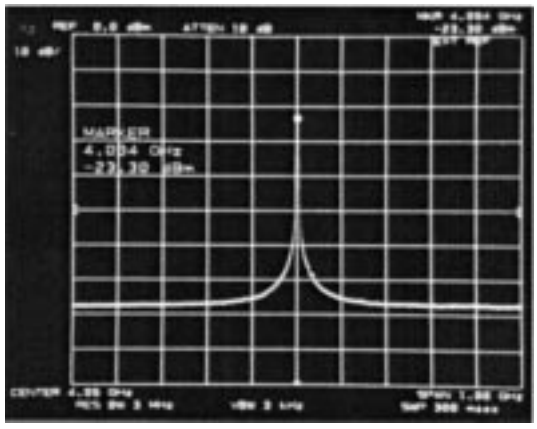
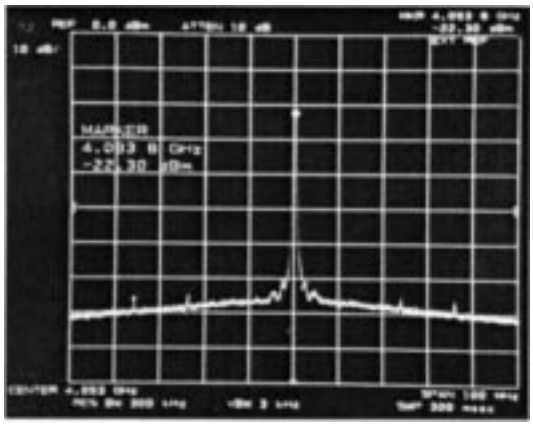


Fig. 13. Chip photo of fabricated CDR IC using scaled HBT process.



(a)



(b)

Fig. 14. Measured performance of the single-chip CDR. (a) Measured free-running VCO at 4 GHz. (b) Recovered clock phase-locked at 4 GHz.

output jitter compared to a single flip-flop implementation of the phase detector [4]. A simplified schematic of the D-type flip-flop is shown in Fig. 11(b), which consists of two current sources generated by an on-chip bias circuit. Each current source is 0.32 mA, resulting in a flip-flop power consumption

of 1.6 mW. The decision circuit retimed the data using a D-type flip-flop which was clocked by the VCO output. The D-type flip-flop was identical to the one used in the phase-detector circuit.

The VCO function was implemented using an *RC* multivibrator with on-chip timing capacitor, a simplified schematic of which is shown in Fig. 12. The on-chip timing capacitor was 25 fF and was implemented by metal–nitride–metal capacitors. All transistors in the VCO design had an emitter area of 0.5 μm^2. The VCO free-running frequency could be controlled using an external voltage.

The CDR chip was designed (see Fig. 13) for on-wafer characterization using a probe card. In all the measurements, the CDR was driving a load of approximately 25 Ω (50 Ω internal in parallel with 50 Ω external). Measurements were performed with a single 2.5-V negative supply and the chip (including input and output buffers) consumed a total dc power of 50 mW. If the CDR is integrated in a front-end system with other circuit functions, the total power is further reduced by eliminating input/output buffers. In this case, the CDR itself consumed only 22 mW of dc power. To our knowledge, this is the lowest power CDR reported at this frequency range. Under this bias condition, the free-running VCO frequency [shown in Fig. 14(a)] was measured at 4 GHz. This test was done without applying any input signal to the chip. The VCO center frequency could be controlled externally over a range of approximately $\pm$15% at this bias condition. Under a locking condition, the recovered clock at around 4 GHz is shown in Fig. 14(b).

V. Conclusions

A new processing approach was presented for fabricating submicrometer HBT's on InP substrate. The process is intended for ultra-high-speed circuits with low-power consumption and a very compact chip size. Excellent device dc and RF performance was achieved for devices as small as a 0.3-μm^2 emitter. Integrated circuits were implemented in this new process. As an example, a comparator test chip operating at 40 GHz and an ultra-low-power CDR consuming 22 mW at 4 GHz were presented.

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References

[1] M. Hafizi, "Recent Progress in InP-based HBT technology," in *Compound Semiconductor 1995* (Ins. Phys. Conf. Series. no. 145). Cheju Island, Korea: Institute of Physics, 1996, ch. 5, pp. 631–636.

[2] W. E. Stanchina *et al.*, "An InP-based HBT fab for high-speed digital, analog, mixed-signal, and optoelectronic IC's," in *Tech. GaAs IC Symp. Dig.*, San Diego, CA, Oct. 1995, pp. 31–34.

[3] C. Baringer *et al.*, "3-bit, 8 GSPS flash ADC," in *Proc. Indium Phosphide Rel Mat. Conf.*, Germany, Mar. 1996, pp. 64–67.

[4] M. Soyuer, "A monolithic 2.3 Gb/s 100-mW clock and data recovery circuit in silicon bipolar technology," *IEEE J. Solid-State Circuits*, vol 28, pp. 1310–1313, Dec. 1993.

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